

Appl. No. 10/806,640  
IDS dated February 16, 2007

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): David Jon Hiner et al.  
Assignee: Amkor Technology, Inc.  
Title: METHOD OF MANUFACTURING A SEMICONDUCTOR PACKAGE  
Serial No.: 10/806,640 Filed: March 23, 2004  
Examiner: Carl J. Arbes Group Art 3729  
Unit:  
Docket No.: G0092-6P

Monterey, CA  
February 16, 2007

Mail Stop Issue Fee  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

**INFORMATION DISCLOSURE STATEMENT**  
**UNDER §1.97**

Sir:

Pursuant to 37 C.F.R. §§ 1.56, 1.97 and 1.98, Applicant(s) wish to call the following documents to the attention of the Examiner. At a minimum, this Information Disclosure Statement should be placed in the file pursuant to 37 C.F.R. § 1.97(i).

**U.S. PATENT DOCUMENTS**

|    | DOCUMENT NUMBER | DATE     | NAME             |
|----|-----------------|----------|------------------|
| 1) | 4,806,188       | 02/21/89 | Rellick          |
| 2) | 7,030,469       | 04/18/06 | Mahadevan et al. |

**OTHER DOCUMENTS**

|    |  |
|----|--|
| 1) | Hiner et al., U.S. Patent Application Serial No. 10/992,371, filed on November 18, 2004, entitled "PRINTED WIRING MOTHERBOARD HAVING BONDED INTERCONNECT REDISTRIBUTION MESA"                    |
| 2) | Scanlan et al., U.S. Patent Application Serial No. 11/293,999, filed on December 5, 2005, entitled "SEMICONDUCTOR PACKAGE INCLUDING A TOP-SURFACE METAL LAYER FOR IMPLEMENTING CIRCUIT FEATURES" |

|    |  |
|----|--|
| 3) | Huemoeller et al., U.S. Patent Application Serial No. 11/497,617, filed on August 1, 2006, entitled "BUILDUP DIELECTRIC AND METALLIZATION PROCESS AND SEMICONDUCTOR PACKAGE"                     |
| 4) | Hiner et al., U.S. Patent Application Serial No. 11/595,411, filed November 9, 2006, entitled "SEMICONDUCTOR PACKAGE INCLUDING TOP-SURFACE TERMINALS FOR MOUNTING ANOTHER SEMICONDUCTOR PACKAGE" |

A PTO form 1449 listing these documents is enclosed.

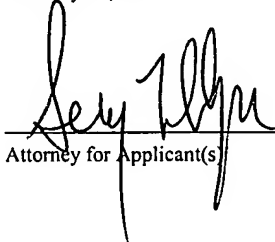
Citation of the above documents shall not be construed as:

1. an admission that the documents are necessarily prior art with respect to the instant invention;
2. a representation that a search has been made, other than as described above; or
3. an admission that the information cited herein is, or is considered to be, material to patentability as defined in § 1.56(b).

The Commissioner is hereby authorized to charge any fees required for consideration of this Information Disclosure Statement, and to credit any overpayment of fees to Deposit Account No. 50-0553.

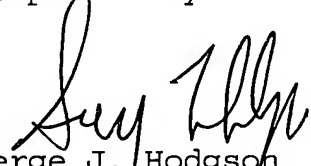
**CERTIFICATE OF MAILING**

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, on February 16, 2007.

  
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Attorney for Applicant(s)

February 16, 2007  
Date of Signature

Respectfully submitted,

  
Serge J. Hodgson  
Attorney for Applicant(s)  
Reg. No. 40,017  
(831) 655-0880



Form PTO-1449

INFORMATION ASSURE CITATION  
IN AN APPLICATION

(Use several sheets if necessary)

Atty Docket No.

G0092-6P

Serial No.

10/806,640

Applicant(s)

David Jon Hiner et al.

Filing Date

March 23, 2004

Group

3729

## U.S. PATENT DOCUMENTS

| EXAMINER<br>INITIAL |    | DOCUMENT NUMBER | DATE     | NAME             | CLASS | SUBCLASS | FILING DATE<br>IF APPROPRIATE |
|---------------------|----|-----------------|----------|------------------|-------|----------|-------------------------------|
|                     | AA | 4,806,188       | 02/21/89 | Rellick          | 156   | 89       |                               |
|                     | AB | 7,030,469       | 04/18/06 | Mahadevan et al. | 257   | 659      |                               |
|                     | AC |                 |          |                  |       |          |                               |
|                     | AD |                 |          |                  |       |          |                               |
|                     | AE |                 |          |                  |       |          |                               |
|                     | AF |                 |          |                  |       |          |                               |
|                     | AG |                 |          |                  |       |          |                               |
|                     | AH |                 |          |                  |       |          |                               |
|                     | AI |                 |          |                  |       |          |                               |
|                     | AJ |                 |          |                  |       |          |                               |

## FOREIGN PATENT DOCUMENTS

|  |    |                 |      |         |       |          | Translation |    |
|--|----|-----------------|------|---------|-------|----------|-------------|----|
|  |    | DOCUMENT NUMBER | DATE | COUNTRY | CLASS | SUBCLASS | YES         | NO |
|  | AK |                 |      |         |       |          |             |    |
|  | AL |                 |      |         |       |          |             |    |
|  | AN |                 |      |         |       |          |             |    |
|  | AM |                 |      |         |       |          |             |    |

## OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

|    |  |
|----|--|
| AO | Hiner et al., U.S. Patent Application Serial No. 10/992,371, filed on November 18, 2004, entitled "PRINTED WIRING MOTHERBOARD HAVING BONDED INTERCONNECT REDISTRIBUTION MESA"                    |
| AP | Scanlan et al., U.S. Patent Application Serial No. 11/293,999, filed on December 5, 2005, entitled "SEMICONDUCTOR PACKAGE INCLUDING A TOP-SURFACE METAL LAYER FOR IMPLEMENTING CIRCUIT FEATURES" |
| AQ | Huemoeller et al., U.S. Patent Application Serial No. 11/497,617, filed on August 1, 2006, entitled "BUILDUP DIELECTRIC AND METALLIZATION PROCESS AND SEMICONDUCTOR PACKAGE"                     |
| AR | Hiner et al., U.S. Patent Application Serial No. 11/595,411, filed November 9, 2006, entitled "SEMICONDUCTOR PACKAGE INCLUDING TOP-SURFACE TERMINALS FOR MOUNTING ANOTHER SEMICONDUCTOR PACKAGE" |

Examiner

Date Considered

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant(s).